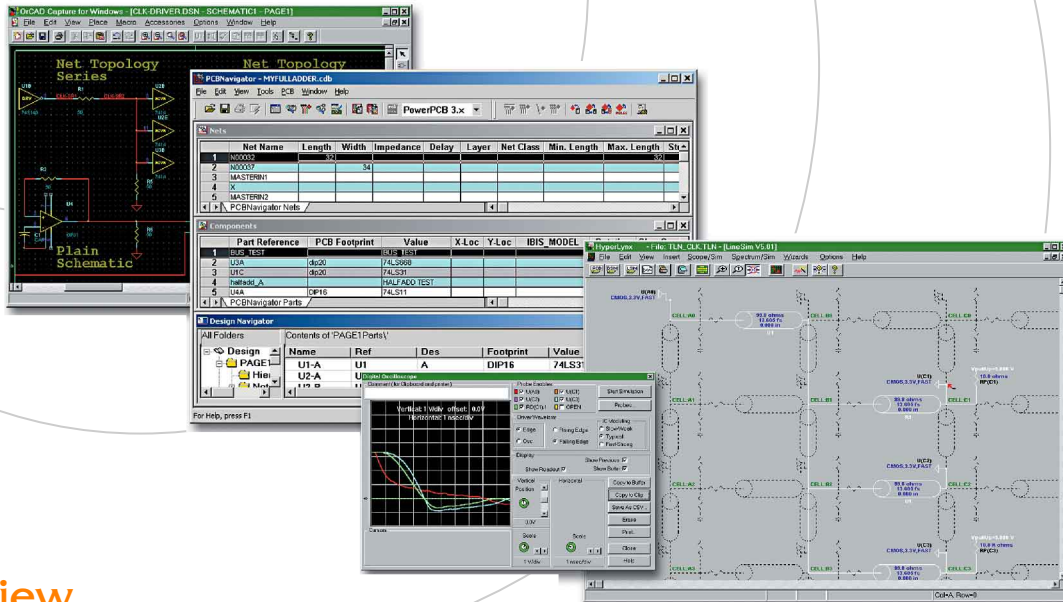


SI-Planner™

Signal Integrity Interconnect Analysis and Design Constraints System



Overview

SI-Planner provides a single integrated environment for planning and optimizing interconnect High-Speed net topologies. Graphical (Capture/View/Draw) What if analysis can be performed quickly to explore critical signals, by simulating net topologies? Signal constraints are generated from LineSim(r) to drive downstream physical design PCB tools, for optimum routing and placement. SI-Planner manages user constraints in a spreadsheet based system, and feed forwards into LineSim(r) for optimizing and PCB routing tools via netlist. The net topologies can be graphically drawn, for what-if analysis or automatically generated from an existing schematic design.

Product Highlights

- ⊕ Reads OrCAD/Innoveda Schematic files and generates net topologies for optimum routing constraints.
- ⊕ Graphical what-if analysis, for building net topologies.
- ⊕ Constraint Planning Management Spread sheet provides total user control over PCB design rules. Supports Board, Net, Pin, and Component design rules attribute information and filters into target PCB systems.
- ⊕ Integrated LineSim(r) 2-D transmission line and crosstalk analysis for generating accurate NET constraints. This option is provided with the SI-Planner Studio package.
- ⊕ Accurate driver/receiver/termination selection.
- ⊕ Supports flat and hierarchical designs.
- ⊕ Perform termination analysis, and builds accurate delay, termination schemes, using LineSim(r).

Benefits of SI-Planner™

- ⊕ Reduce PCB board turns due to excessive signal delays caused by ringing, crosstalk and incorrect design rules.
- ⊕ Saves up to 50% in labor compared to manual method. No need to guess or memorize PCB router design rules.
- ⊕ Maintain design integrity between OrCAD/Innoveda schematic designs and target PCB Systems through back annotation of ECO changes in PCB layout. Supported PCB Systems are, PADS, Accel-EDA, Mentor, Cadence, Zuken-Redac, and Expedition.
- ⊕ Analyze Drivers/Receivers on a Node: NET topology spreadsheet viewer, transfer to LineSim(r).
- ⊕ Assign multiple design rules for nets (HS Rules), components (clusters), and board (track2track, etc.)

